

PCI-EXPRESS EDGE CONNECTOR

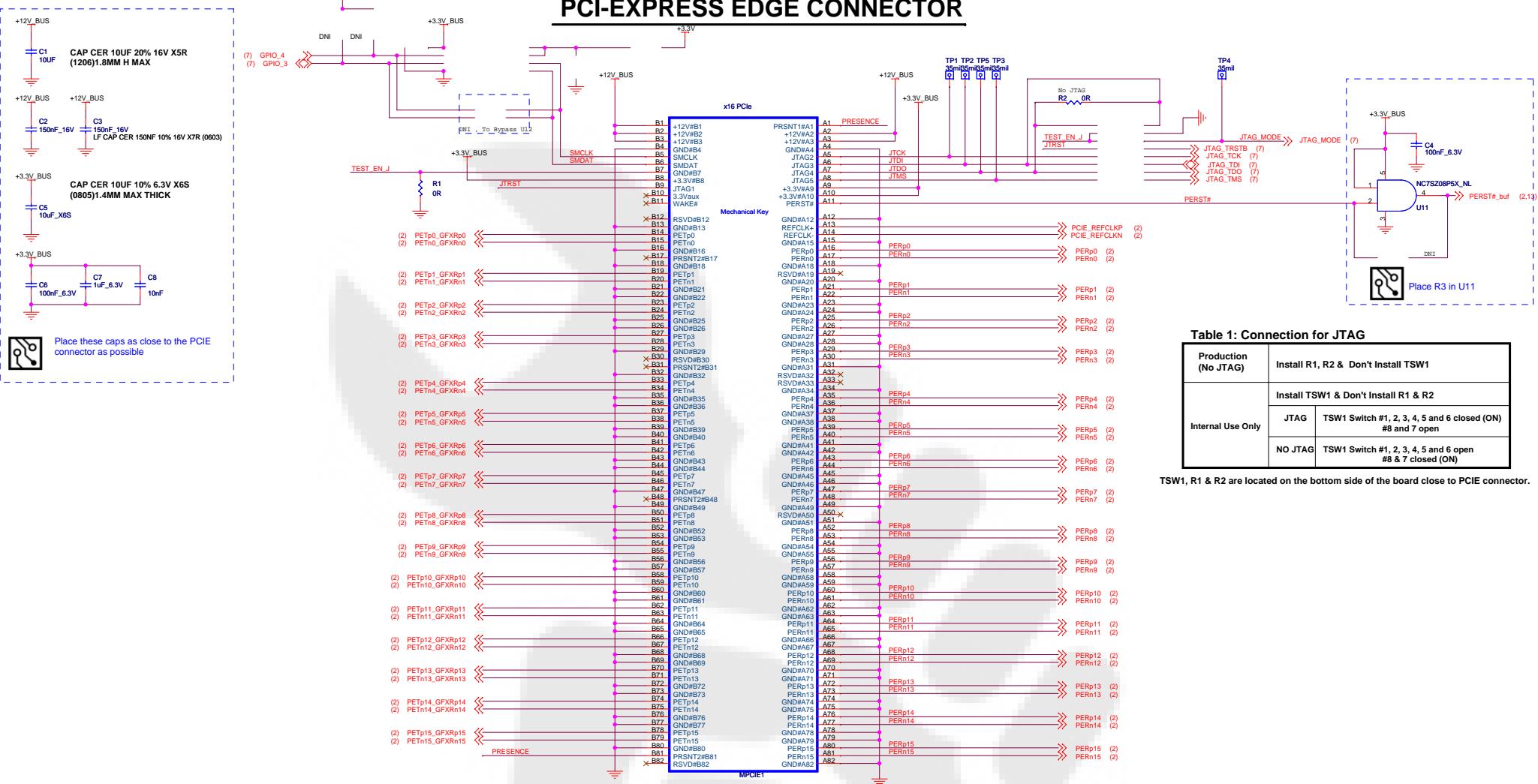


Table 1: Connection for JTAG

| Production (No JTAG) | Install R1, R2 & Don't Install TSW1 | |
|-------------------------|-------------------------------------|---|
| Internal Use Only | JTAG | TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open |
| | NO JTAG | TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON) |
| | | |

TSW1, R1 & R2 are located on the bottom side of the board close to PCIe connector.

| SYMBOL LEGEND | |
|---------------|----------------|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |
| BUO | BRING UP ONLY |

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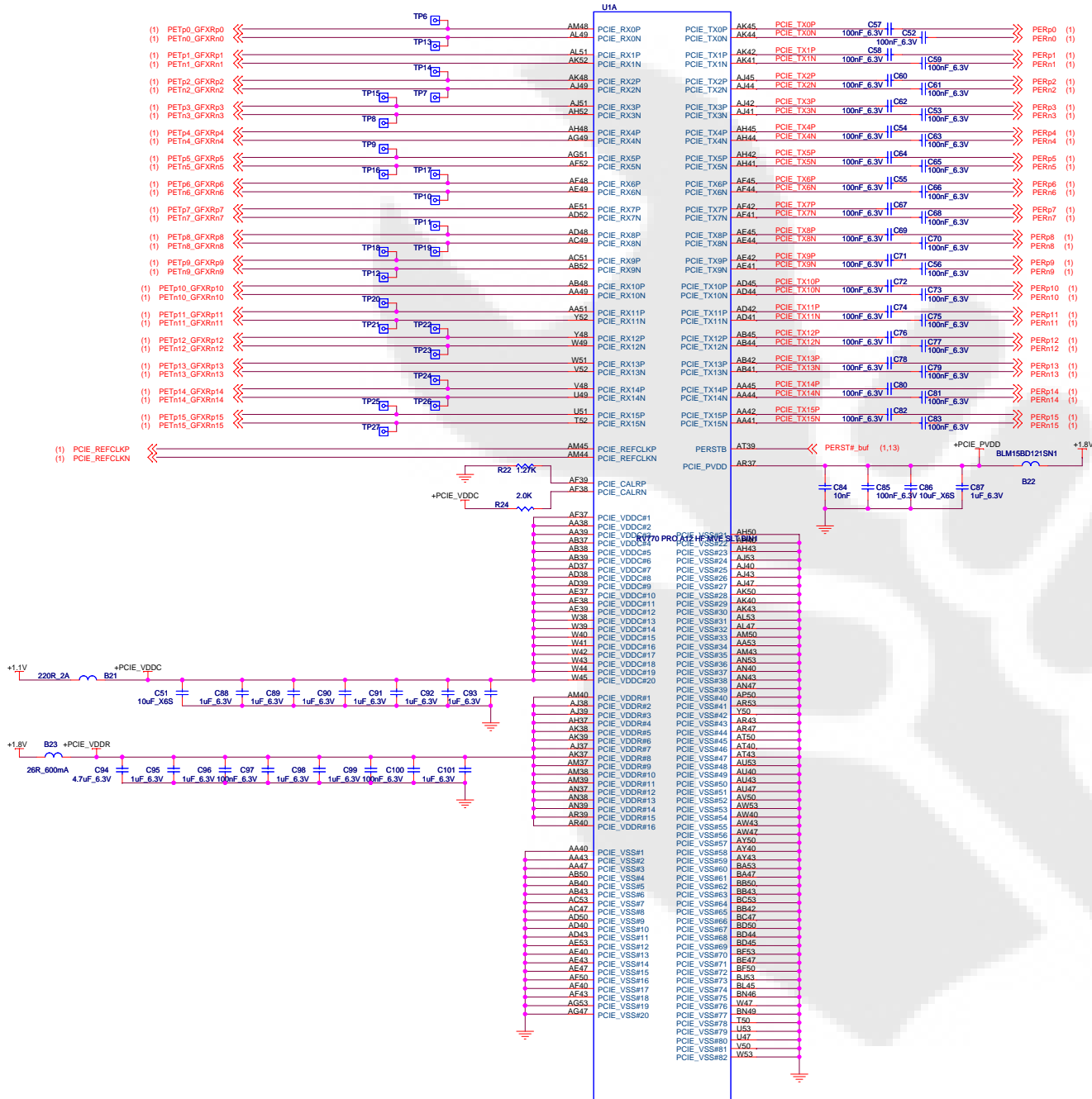
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Rev 25

Sheet 1 of 21

File RH_PCIE_RV770_512MB_GDDR3_QUAD_40450762.FLT

NOTE: some of the PCIe testpoints will be available through via on traces.

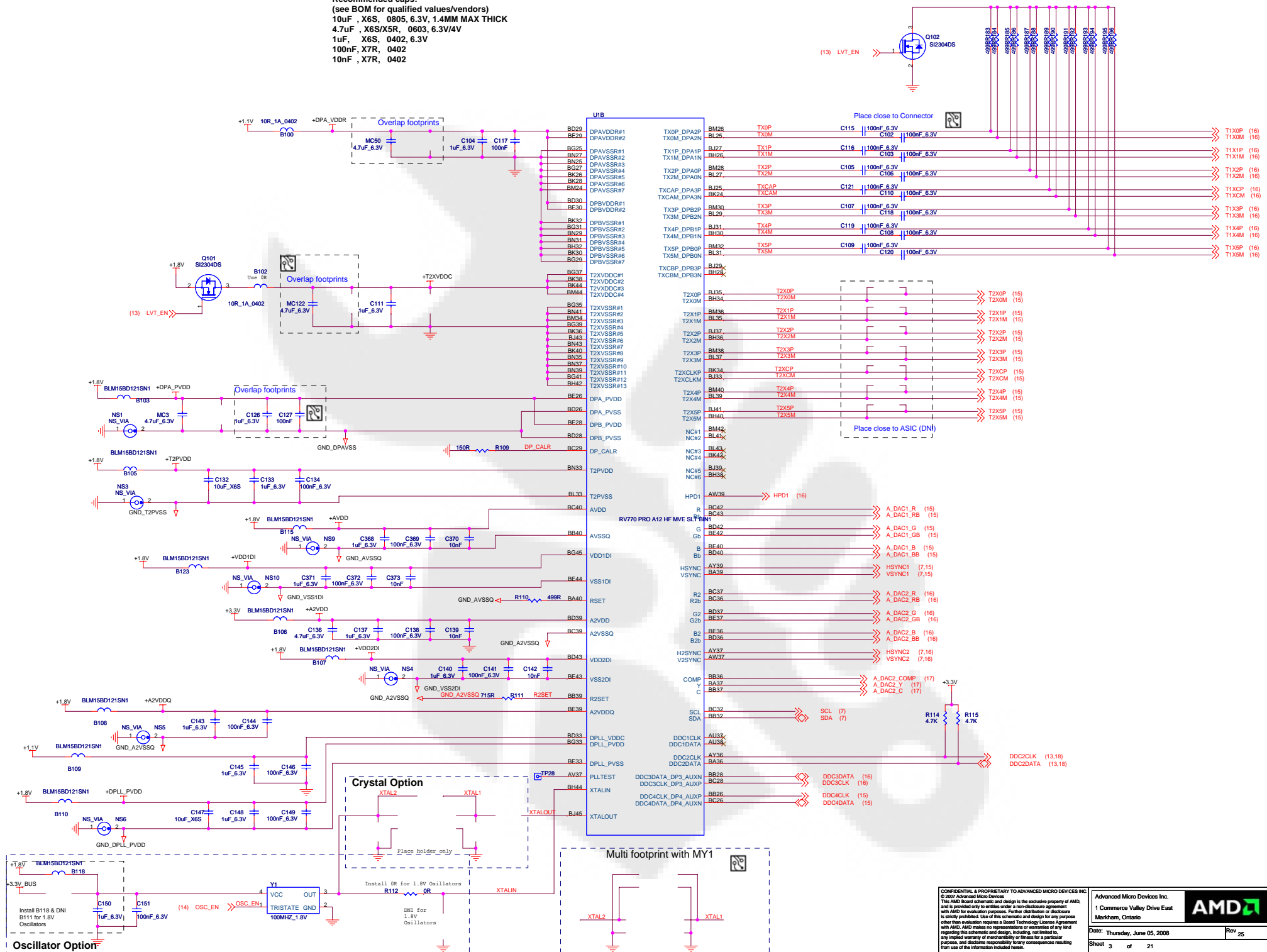


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
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Rev: 25
Sheet 2 of 21

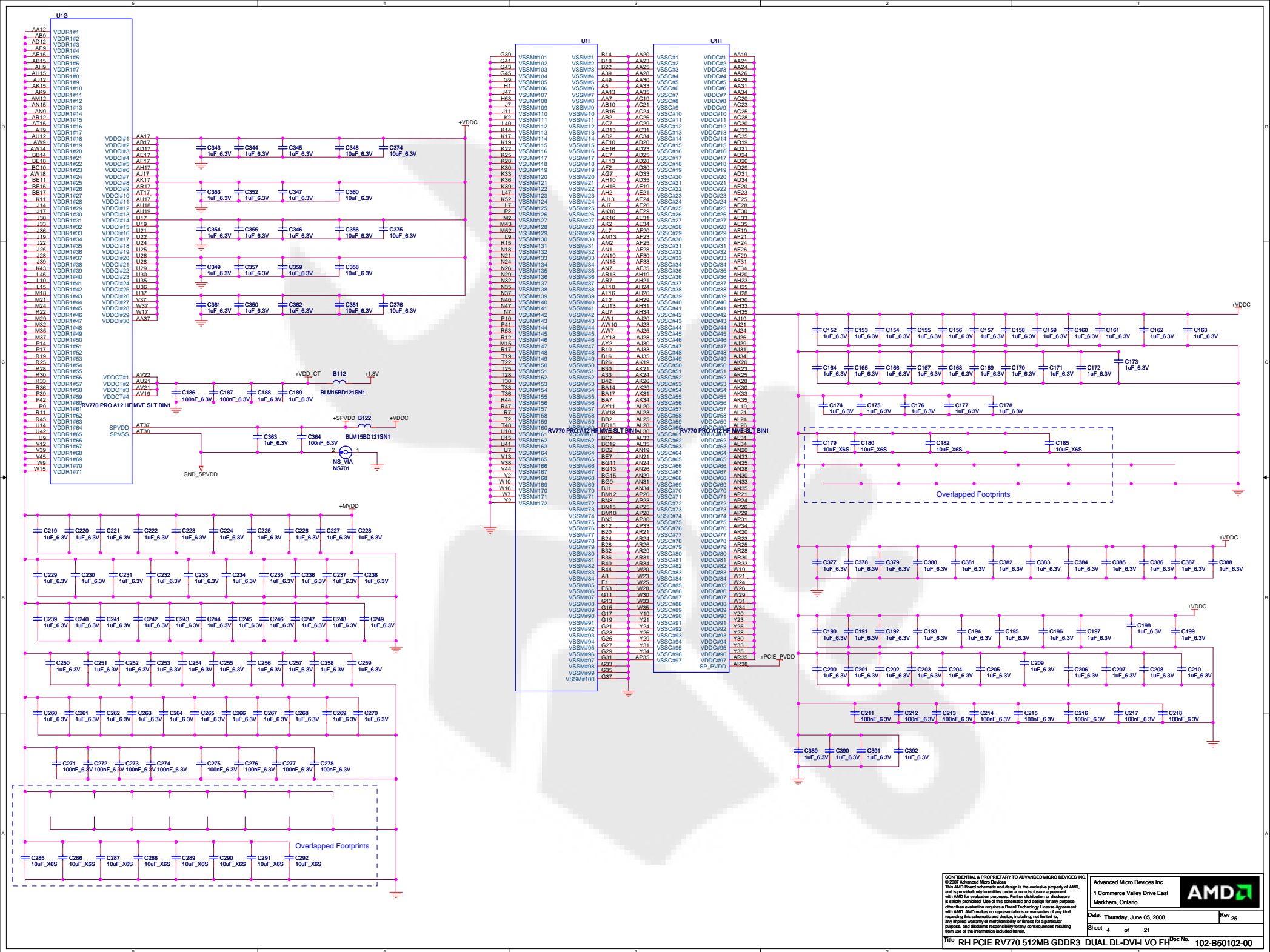


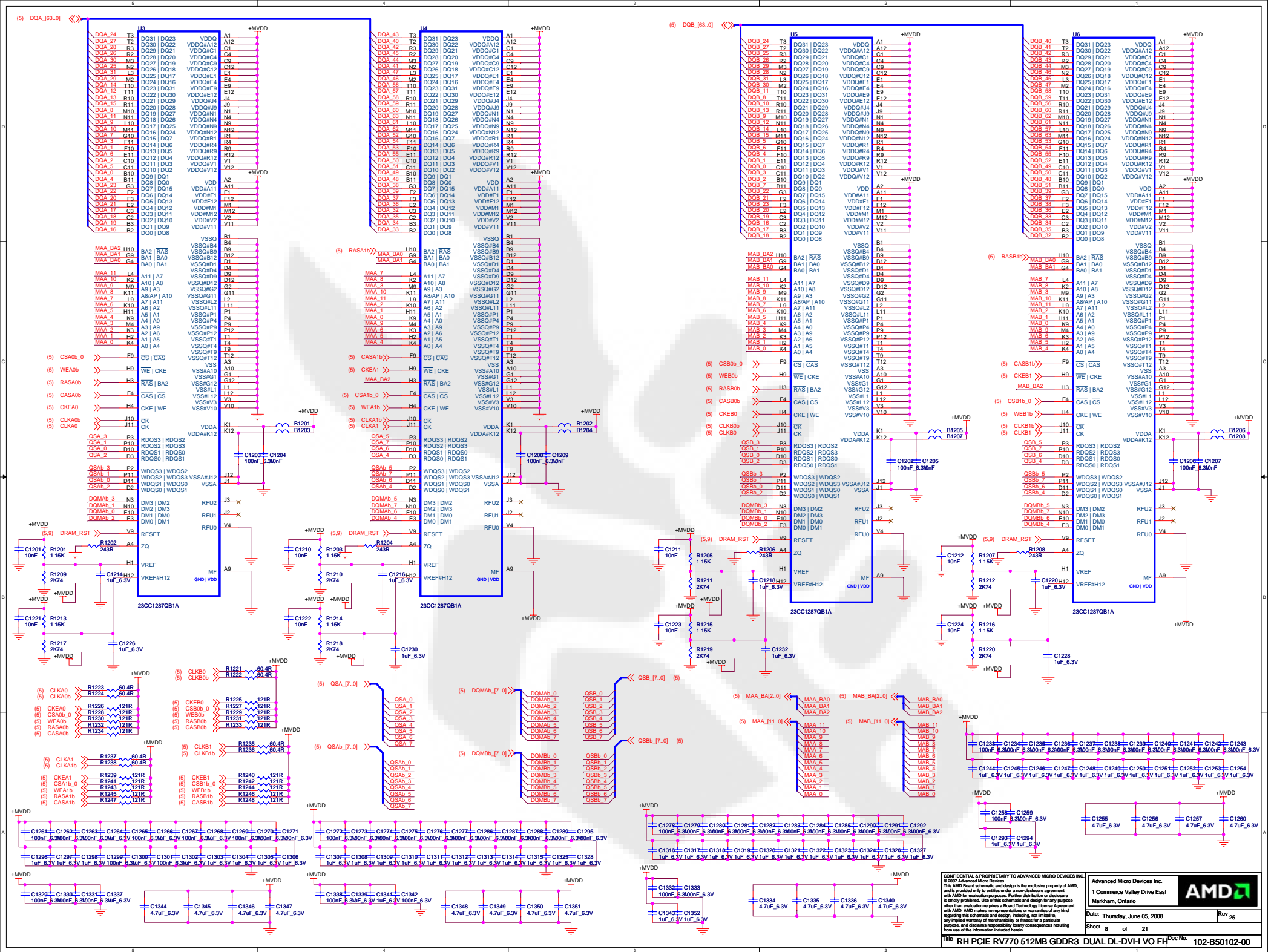
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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| Date: Thursday, June 05, 2008 | | Rev 25 | |
| Sheet 3 of 21 | | | |
| DUAL DL-DVI-I VO FH | | Doc No. 102-B50102-00 | |







| U1J | | | |
|-----------------|------------|----------|-----------------|
| BK49 | SP_RX0P | SP_TX0P | BH48 |
| BL51 | SP_RX0N | SP_TX0N | BH49 |
| BL50 | SP_RX1P | SP_TX1P | BC45 |
| BG52 | SP_RX1N | SP_TX1N | BC44 |
| BF48 | SP_RX2P | SP_TX2P | BB45 |
| BE49 | SP_RX2N | SP_TX2N | BB44 |
| BE51 | SP_RX3P | SP_TX3P | AV42 |
| BD52 | SP_RX3N | SP_TX3N | AT43 |
| BD48 | SP_RX4P | SP_TX4P | AV45 |
| BC49 | SP_RX4N | SP_TX4N | AV44 |
| BC51 | SP_RX5P | SP_TX5P | AW42 |
| BS52 | SP_RX5N | SP_TX5N | AW41 |
| BS48 | SP_RX6P | SP_TX6P | AW45 |
| BA49 | SP_RX6N | SP_TX6N | AW44 |
| BA51 | SP_RX7P | SP_TX7P | AU42 |
| AV52 | SP_RX7N | SP_TX7N | AU41 |
| AV48 | SP_RX8P | SP_TX8P | AU45 |
| AW49 | SP_RX8N | SP_TX8N | AU44 |
| AW51 | SP_RX9P | SP_TX9P | AT42 |
| AV52 | SP_RX9N | SP_TX9N | AT41 |
| AV48 | SP_RX10P | SP_TX10P | AT45 |
| AU49 | SP_RX10N | SP_TX10N | AT44 |
| AU51 | SP_RX11P | SP_TX11P | AR42 |
| AT52 | SP_RX11N | SP_TX11N | AR41 |
| AT48 | SP_RX12P | SP_TX12P | AR45 |
| AR49 | SP_RX12N | SP_TX12N | AR44 |
| AR51 | SP_RX13P | SP_TX13P | AN42 |
| AF52 | SP_RX13N | SP_TX13N | AN41 |
| AP48 | SP_RX14P | SP_TX14P | AN45 |
| AN49 | SP_RX14N | SP_TX14N | AN44 |
| AN51 | SP_RX15P | SP_TX15P | AM42 |
| AM52 | SP_RX15N | SP_TX15N | AM41 |
| BM47 | SP_REFCLKP | SP_CALRP | AH38 |
| BK46 | SP_REFCLKN | SP_CALRN | AH39 |

RV770 PRO A12 HF MVE SLT BIN1

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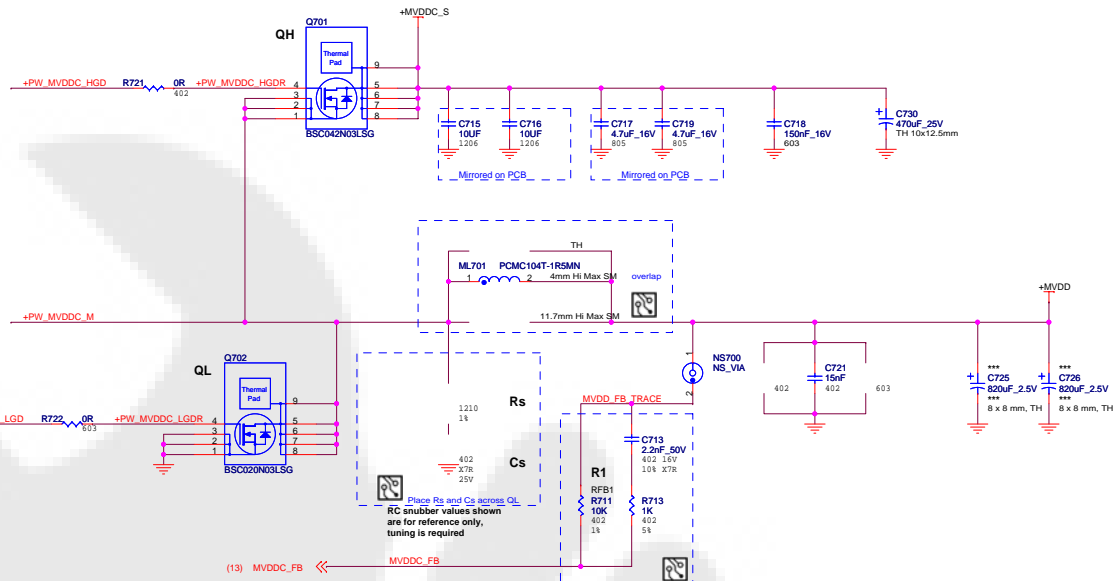
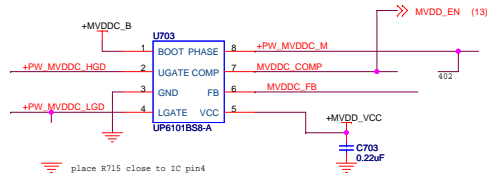
Date: Thursday, June 05, 2008

Sheet 10 of 21

Title RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO F

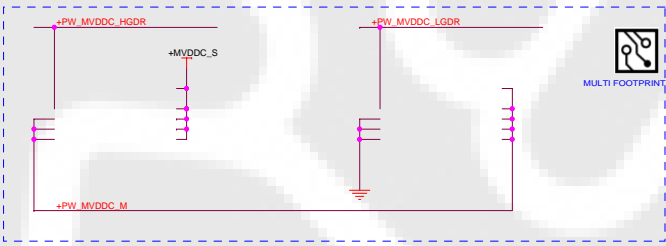
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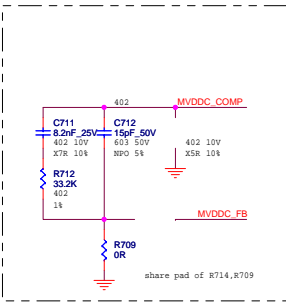


Layout guideline

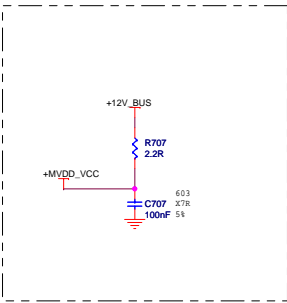
- 1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
- 2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:
Vcc bypass cap is C703, and Boost cap is C705.
- 3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R715, C711 and C712.



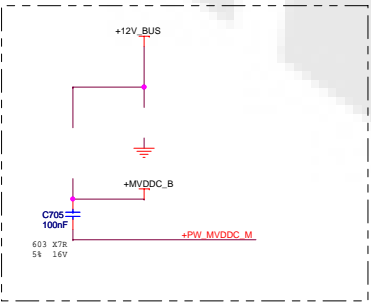
COMPENSATION CIRCUIT



FILTERED SMPS VCC

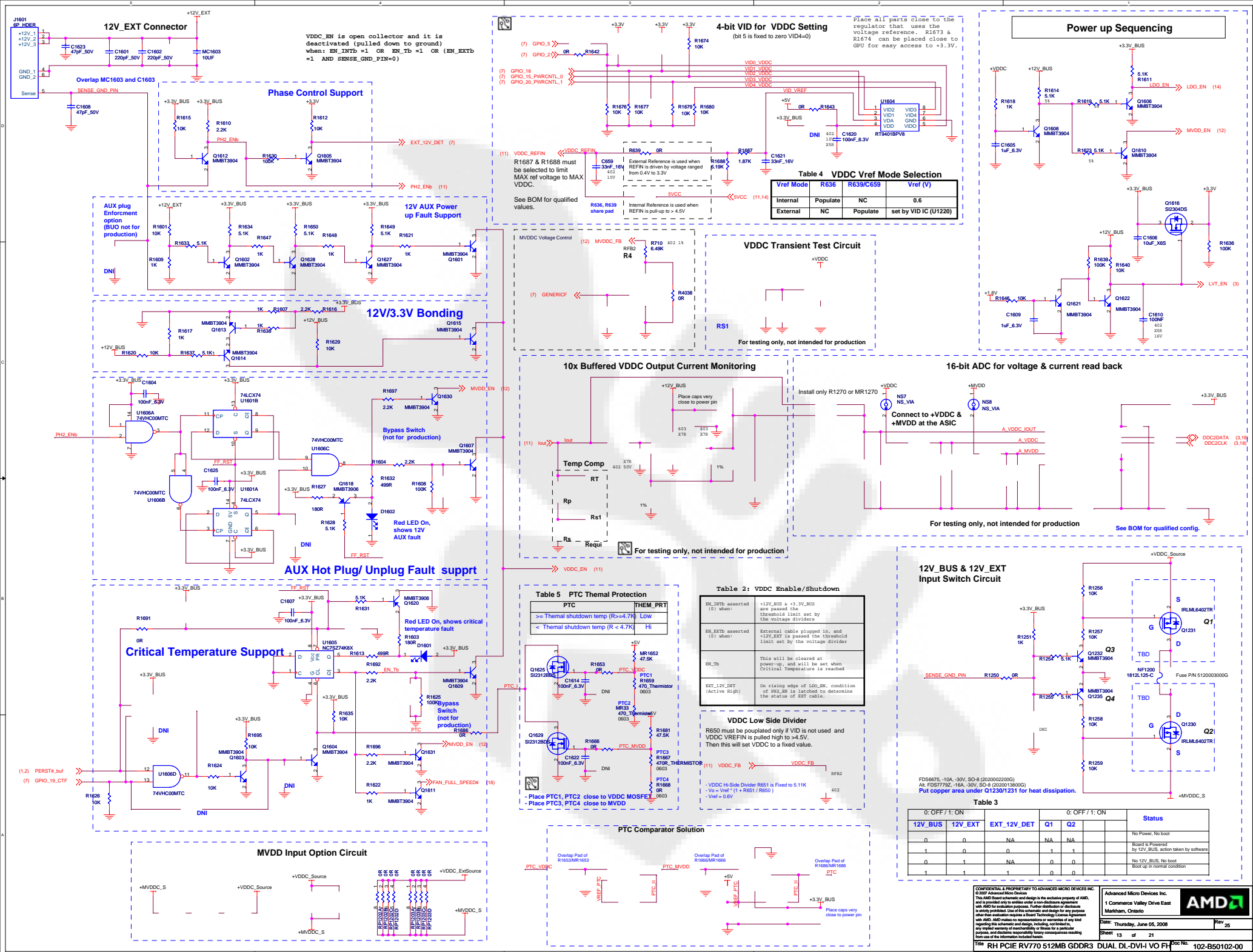


BOOT CIRCUIT



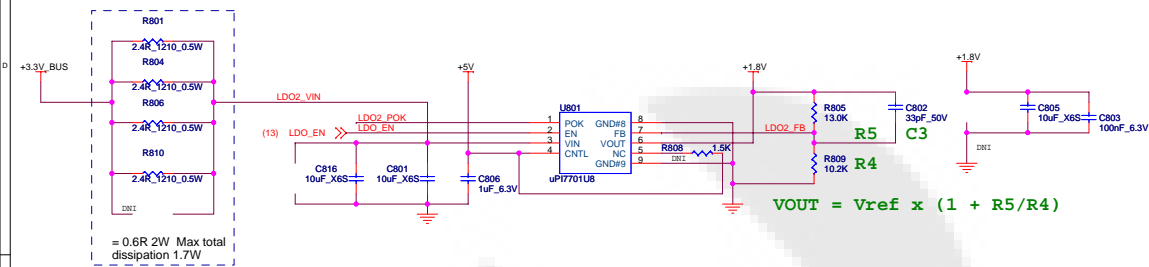
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| Date: Thursday, June 05, 2008 Sheet 12 of 21 | Rev 25 | |
| Title RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FPC No. 102-B50102-00 | | |

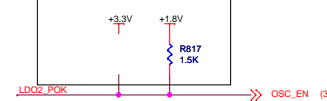


LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling

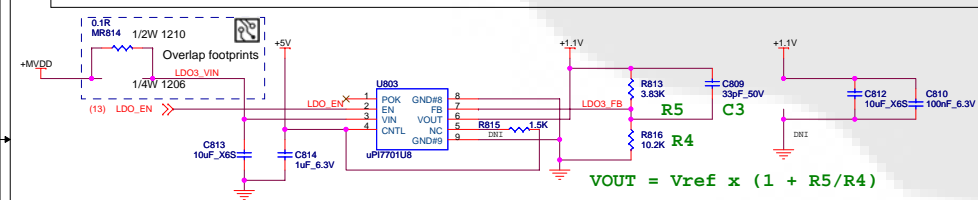


Install R817 if Y1 is a 1.8V Device
Install R807 if Y1 is a 3.3V Device

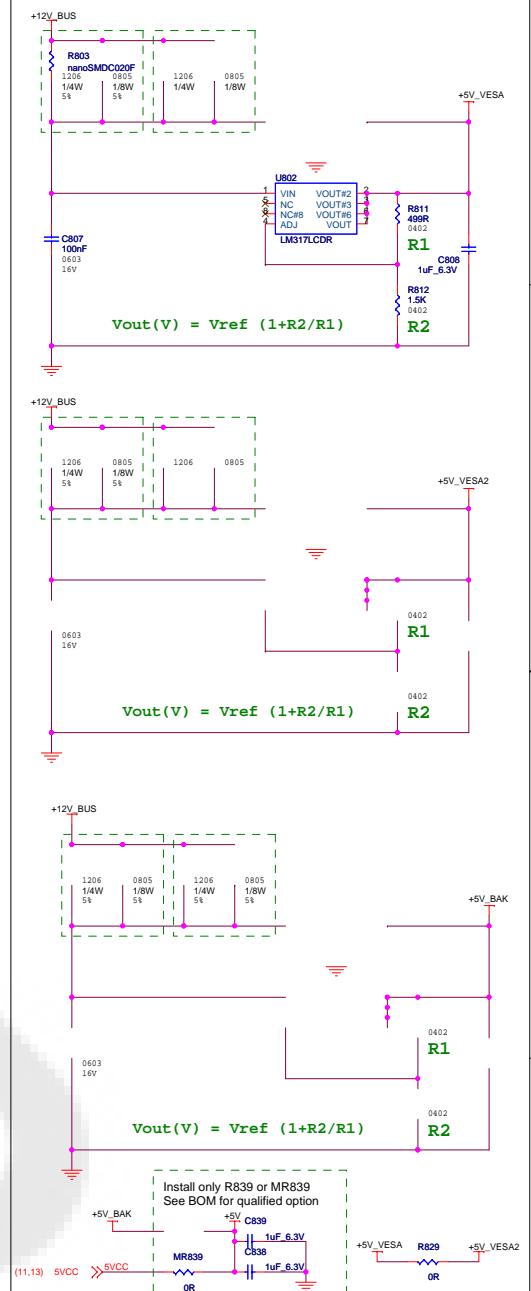


LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling



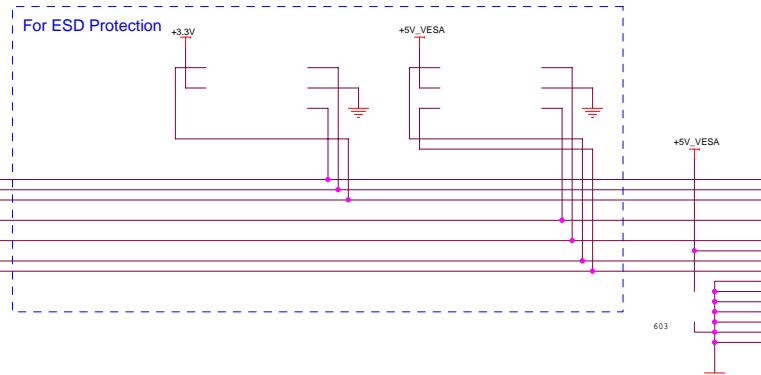
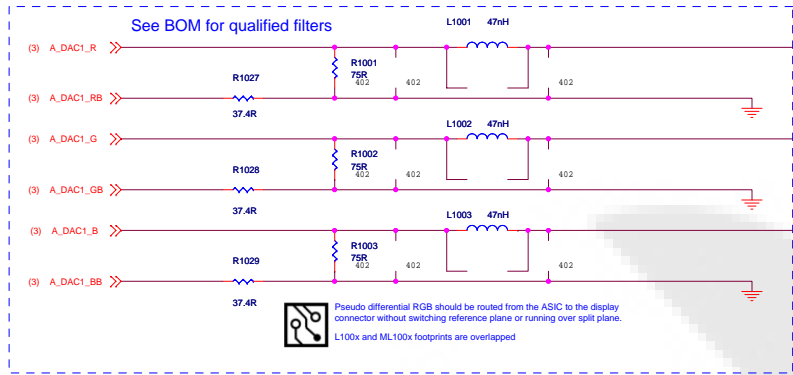
Regulators for +5V, +5V_VESA and +5V_VESA2



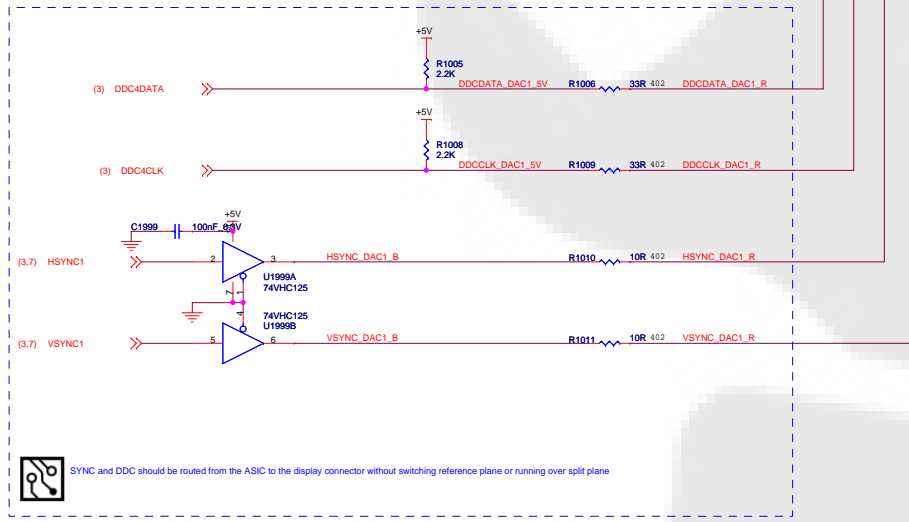
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Date: Thursday, June 05, 2008
Sheet 14 of 21
Rev 25

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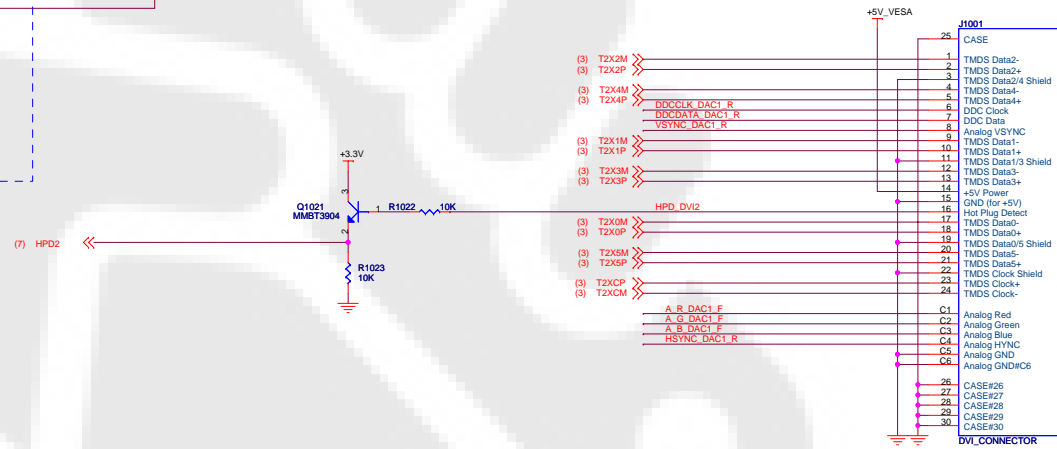


DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)



| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|------------------|------------------|--------------------|----------------------|---------------------|----------------|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | Optional |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | Optional |
| 9 | N/C | +5V | +5V | +5V | Optional |
| Hardware Support | No | Yes | Yes | No | Yes |
| | | 50mA min 1A max | 50mA min 1A max | 300mA min 1A max | |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



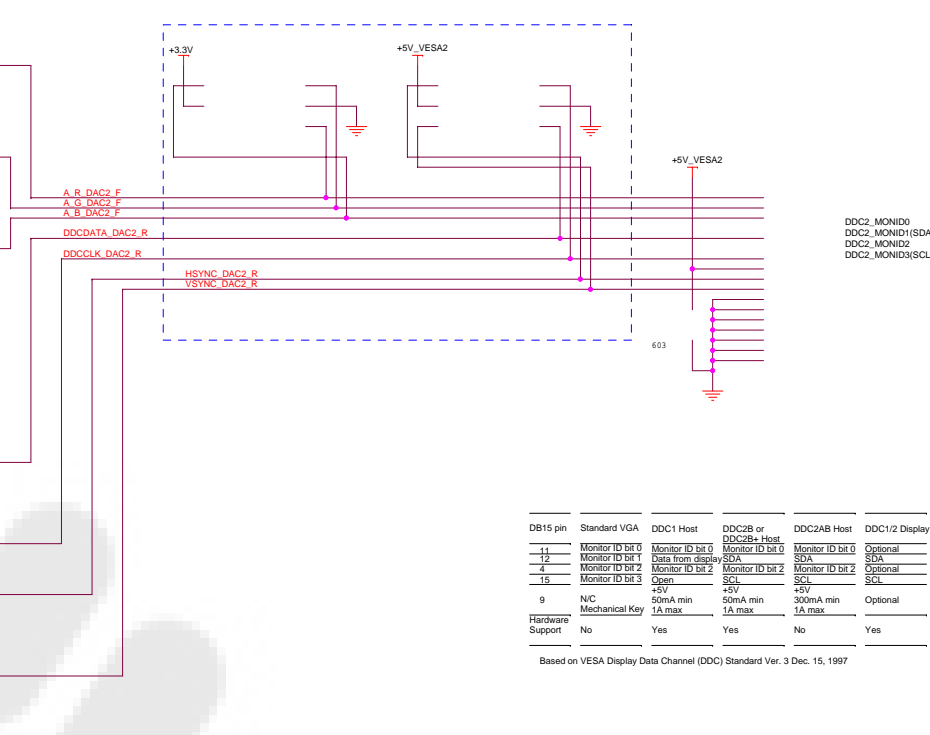
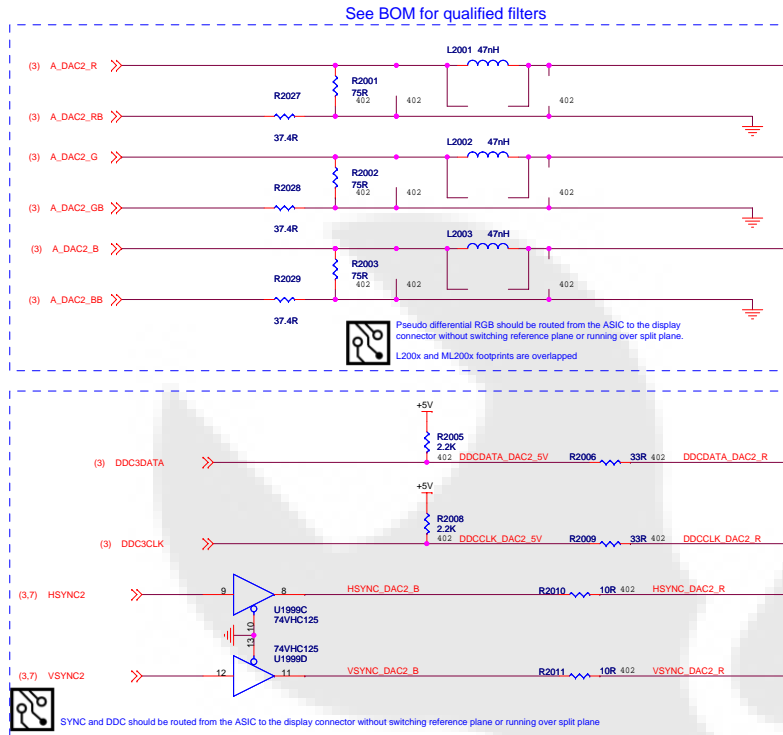
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Sheet 15 of 21

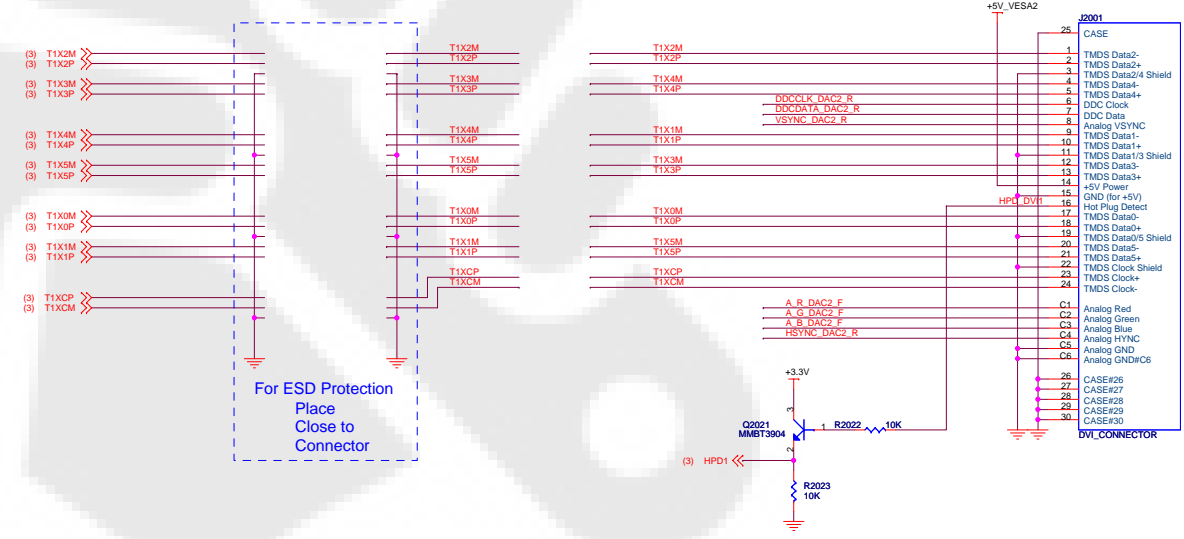
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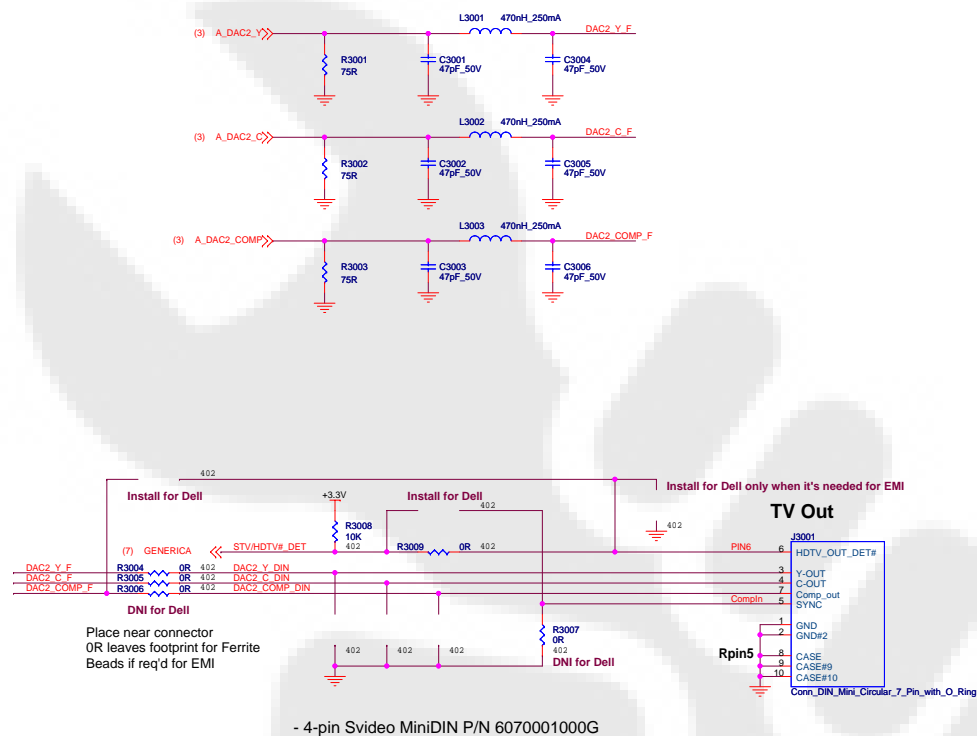
Title RH PCIe RV770 512MB GDDR3 DUAL DL-DVI-I VO Fw Pch No. 102-B50102-00



| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|------------------|------------------|--------------------|----------------------|---------------------|----------------|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | Optional |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | Open | Open | Optional |
| 9 | N/C | +5V | +5V | +5V | Optional |
| Hardware Support | No | Yes | Yes | No | Yes |
| | | 50mA min 1A max | 50mA min 1A max | 300mA min 1A max | |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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Doc No. 102-B50102-00

Sheet 17 of 21

Rev 25

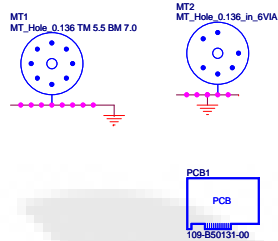
Title RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FH

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>



PCIE 12V/3.3V Power up Bonding support

BKT1: DS, DVI-I DIN - DVI

BKT2
BRACKET
8020038600G



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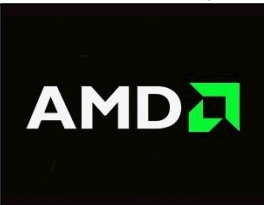
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Sheet 19 of 21

Rev 25



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| Title |
|---|
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Schematic No.
102-B50102-00

Date:
Thursday, June 05, 2008

REVISION HISTORY

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 Please contact AMD representative to obtain latest BOM closest to the application desired.

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